WHAT IS CLAIMED IS:

1. A circuit arrangement for generating test-traffic on a digital data path having at least one other traffic source, comprising:

a data-generation circuit adapted to provide a first data stream;

a memory arrangement adapted to buffer a plurality of programmable commands, the programmable commands indicative of at least one of test-traffic type, pattern and behavior-in-time;

state machine circuitry coupled between the memory arrangement, the data-generation circuit and the digital data path, the state machine circuitry adapted to assemble portions of the first data stream into test-traffic wherein at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands, and further adapted to generate test-traffic on the digital data path; and

a status and feedback circuit adapted to monitor the digital data path for test-traffic and generate a feedback signal indicative of at least one of test-traffic throughput and test-traffic quality.

2. The circuit arrangement of claim 1, wherein

the state machine circuitry includes a command state machine and a bus master state machine, the command state machine being coupled to the memory arrangement and data-generation circuit, and adapted to direct the bus master state machine to assemble portions of the first data stream into test-traffic having pre-defined type, pattern and behavior-in-time responsive to the programmable commands, and

the bus master state machine is coupled to the digital data path and adapted to communicate the test-traffic onto the digital data path responsive to the command state machine.

3. The circuit arrangement of claim 1, wherein the state machine circuitry is adapted to assemble portions of the first data stream into a test-traffic type selected from a group consisting of 1, 2, 4, 8, 16, 32, and 64 words per burst.

4. The circuit arrangement of claim 1, wherein the state machine circuitry is adapted to assemble portions of the first data stream into a test-traffic type selected from a group consisting of other than 1, 2, 4, 8, 16, 32, and 64 transfers per burst.

5. The circuit arrangement of claim 1, wherein the state machine circuitry is further adapted to receive the first data stream from the data-generation circuit without generating test-traffic on the digital data path.

6. The circuit arrangement of claim 1, wherein the state machine circuitry is adapted to pause in response to programmable commands.

7. The circuit arrangement of claim 1, further comprising a bus interface circuit coupled between the memory arrangement and the digital data path, the bus interface circuit adapted to pass programmable commands received via the digital data path to the memory arrangement.

8. The circuit arrangement of claim 1, wherein the first data stream is a repeatable sequence of binary data.

9. The circuit arrangement of claim 8, wherein the data-generation circuit is a second memory arrangement, the first data stream being stored in the second memory arrangement.

10. The circuit arrangement of claim 8, wherein the first data stream comprises a sequence of pseudo-random numbers.

11. The circuit arrangement of claim 10, wherein the data-generation circuit is a second memory arrangement, the first data stream being stored in the second memory arrangement.

12. The circuit arrangement of claim 10, wherein the data-generation circuit is a linear feedback shift register (LFSR) circuit, the first data stream comprising a sequence of LFSR values.

13. The circuit arrangement of claim 12, wherein the state machine circuitry is configured and arranged to seed the LFSR and control content of the first data stream.

14. The circuit arrangement of claim 13, wherein the status and feedback circuit is further adapted to verify monitored test-traffic against corresponding LFSR values, and the feedback signal being an interrupt generated indicative of the test-traffic verification.

15. The circuit arrangement of claim 1, wherein the status and feedback circuit is further adapted to verify monitored test-traffic against a corresponding first data stream, and the feedback signal being an interrupt generated indicative of the test-traffic verification.

16. The circuit arrangement of claim 15, wherein the memory arrangement includes command registers adapted to store programmable commands, configuration registers adapted to store traffic generation process control information and status registers adapted to store test-traffic verification information.

17. The circuit arrangement of claim 1, wherein the status and feedback circuit includes a counter adapted to specify a number of command repetitions, and a loop timer adapted to specify a period within which a set of programmable commands must execute.

18. The circuit arrangement of claim 1, wherein the digital data path is an AHB protocol bus.

19. A computer system, comprising:

a digital data path;

a plurality of traffic sources, each traffic source coupled to the digital data path and adapted to communicate non-test-traffic onto the digital data path; and

a circuit arrangement for generating test-traffic coupled to the digital data path, the circuit arrangement including,

a data-generation circuit adapted to provide a first data stream,

a memory arrangement adapted to buffer a plurality of programmable commands, the programmable commands indicative of at least one of test-traffic type, pattern and behavior;

state machine circuitry coupled between the memory arrangement, the data-generation circuit and the digital data path, the state machine circuitry adapted to assemble portions of the first data stream into test-traffic wherein at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands, and further adapted to generate test-traffic on the digital data path; and

a status and feedback circuit adapted to monitor the digital data path for test-traffic and generate a feedback signal indicative of at least one of test-traffic throughput and test-traffic quality, wherein at least one of the plurality of traffic sources is a processor circuit.

20. The circuit arrangement of claim 19, wherein the data-generation circuit is a linear feedback shift register (LFSR) circuit, the first data stream consists of a sequence of pseudo-randomly generated binary numbers representing LFSR values.

21. The circuit arrangement of claim 20, wherein the status and feedback circuit is further adapted to verify monitored test-traffic against a corresponding first data stream, and the feedback signal is an interrupt generated indicative of the test-traffic verification.

22. A method of generating test-traffic on a digital data path having at least one other traffic source, comprising:

coupling a dedicated test-traffic source to the digital data path;

providing a first data stream, the first data stream being replicatable;

storing a plurality of programmable commands, the programmable commands indicative of at least one of test-traffic type, pattern and behavior;

assembling portions of the first data stream into test-traffic wherein at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands;

generating test-traffic on the digital data path;

monitoring the digital data path for the test-traffic;

verifying the monitored test-traffic against a corresponding first data stream; and

generating a feedback signal indicative of the test-traffic verification.

23. The method of claim 22, wherein the first data stream is a sequence of pseudo-random numbers each representative of a linear feedback shift register (LFSR) value.

24. The method of claim 23, further comprising, verifying monitored test-traffic against a corresponding LFSR value, wherein the feedback signal is an interrupt indicative of each test-traffic verification.

25. The method of claim 22, further comprising:

counting a pre-determined number of command-execution repetitions;

timing each command-execution repetition against an associated programmable period; and

generating a feedback signal indicative a command-execution repetition exceeding the associated programmable period.

26. The method of claim 22, wherein the digital data path is an AHB protocol bus.

27. The method of claim 26, wherein

test-traffic type is one of a group consisting of 1, 2, 4, 8, 16, 32, and 64 transfers per burst.

28. A circuit arrangement for generating test-traffic on a digital data path having at least one other traffic source, comprising:

means for coupling a dedicated test-traffic source to the digital data path;

means for providing a first data stream, the first data stream being replicatable;

means for storing a plurality of programmable commands, the programmable commands indicative of at least one of test-traffic type, pattern and behavior;

means for assembling portions of the first data stream into test-traffic wherein at least one of type, pattern and behavior-in-time is selected responsive to the programmable commands;

means for generating test-traffic on the digital data path;

means for monitoring the digital data path for the test-traffic;

means for verifying the monitored test-traffic against a corresponding first data stream; and

means for generating a feedback signal indicative of the test-traffic verification.